JK FLIPFLOP

module JKFF(input J,input K, input clk, input rst,output reg Q);

always @(posedge clk or posedge rst)

begin

if(rst == 1)

begin

Q <= 0;

end

else

begin

case({J, K})

2'b00: Q <= Q;

2'b01: Q <= 1'b0;

2'b10: Q <= 1'b1;

2'b11: Q <= ~Q;

endcase

end

end

endmodule

TESTBENCH

module JKFF\_tb;

reg J,K,clk,rst;

wire Q;

JKFF JKflipflop(.J(J),.K(K),.clk(clk),.rst(rst),.Q(Q));

initial

begin

clk=0; J = 0;K = 0;

#5 rst = 1;

#30 rst = 0;

$monitor($time, "\tclk=%b\t ,rst=%b\t, J=%b\t,K=%b\t, Q=%b",clk,rst,J,K,Q);

#100 $finish;

end

always

#5 clk = ~clk;

always

#30 J = ~J;

always

#40 K = ~K;

initial

begin

$dumpfile("dump.vcd");

$dumpvars(1);

#10000$finish;

end

endmodule